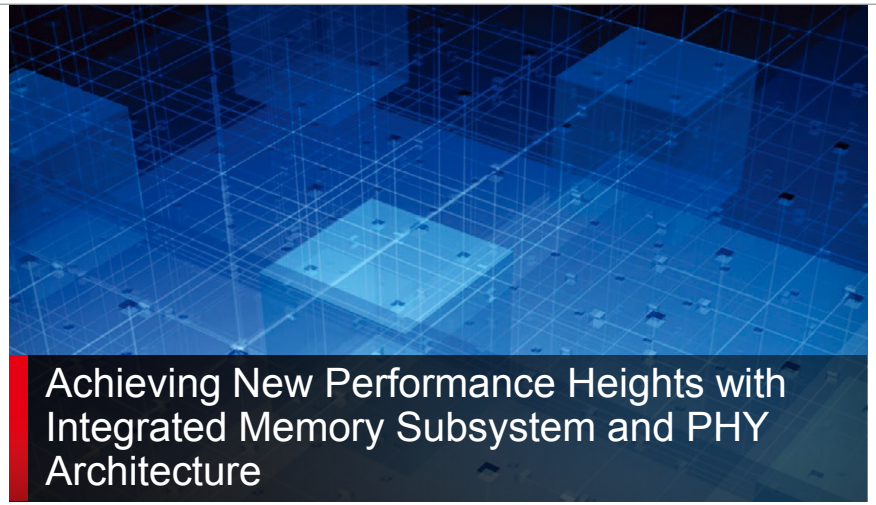
Achieving New Performance Heights with Integrated Memory Subsystem and PHY Architecture

Cadence

ABSTRACT

Next generation mobility products and emerging applications require much higher performance in LPDDR subsystem. This session will cover the implementation of an integrated controller and DDR/LPDDR PHY subsystem, as well as a new scalable DDR/LPDDR PHY architecture. Performance results in 28HPC+, 16FF+ and 16FFC implementation will be presented.



Achieving New Performance Heights with Integrated Memory Subsystem and PHY Architecture

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San Jose, CA
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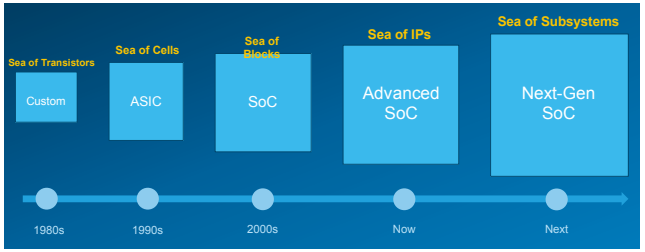
Design Complexity | Analog | Memory Subsystems

SoC Design Challenges
System integration

- SoCs are increasing in system design complexity
- Conflicting requirements to optimize analog elements
- Future SoC requires integration of multiple subsystems



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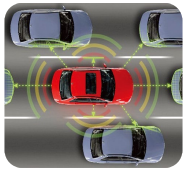
Divergent Optimizations for Different Markets
No one SoC or IP fits all solutions…or does it?

Networking	Mobile/ Consumer	Automotive	Internet of Things
			
• High bandwidth • High performance • Heat dissipation	• Low power • Small area • High data efficiency • Security	• Vision capacity • Complex application development • System integration • Safety, reliability, and security	• Battery life • Lowest cost • Sensor fusion • Wireless • Security

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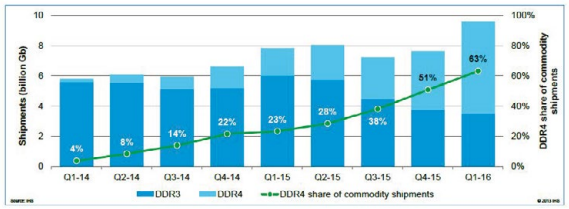
DRAM Market Trends
DDR4 ramp driven by cloud

- 50% bandwidth over DDR3, 20% less energy than DDR3
- Optimized for cloud platforms, high capacity (3D stacking, LRDIMM)
- Cadence wins at many of ARM®-based microserver designs
- 2016 expected for DDR4 to be the dominant memory and extend to other segments



Source: IHS Martkit

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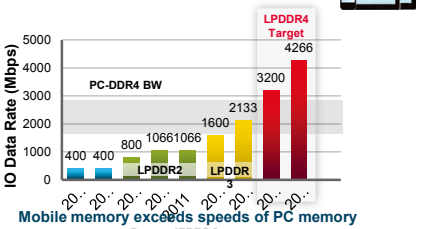
DRAM Market Trends

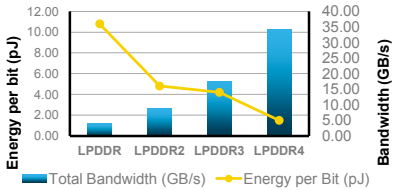
LPDDR4 market introduction

- Mobile AP driving memory bandwidth driven by graphics, gaming, and media apps
- 2X bandwidth over LPDDR3, 50% less energy
- LPDDR4 production in 2015 phones
- Cadence has Tier 1 LPDDR4 subsystem wins in 2014



Mobile memory exceeds speeds of PC memory

Source JEDEC forum



LPDDR4 provides higher bandwidth with lesser energy consumption

Source JEDEC forums

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Low-Power Design

- Modern SoCs demand multiple power requirements

Power Measure	Dominant During	Techniques
Max Dynamic	Heavy Load	Clock Gating, Dynamic Frequency, and Voltage Scaling
Active Leakage	Light Load	VT Selection and Leakage Recovery
Shutdown Leakage	Standby	Power Switch Network Design, Voltage Lowering During Standby

- Different power modes to support several SoC platforms
  - High-end system: High performance, sophisticated LP features
  - Low-cost system: Mainstream performance, cost-efficient LP implementation
- Opposing constraints
  - Meet high-performance goals, such as DDR3200
  - EM/IR targets

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Design Challenges—Leveling

- Optimizes the communication paths between the PHY and DRAM
- Write leveling
  - Align the write DQS with memory clock
- Gate training
  - Place read gate in the preamble
- Read leveling
  - Capture read data in middle of the data valid window
- Write DQ training
  - Allow the DRAM to capture write data in the middle of the data valid window
- Per-bit adjustment is a must at higher data rates

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Design Challenges—Controller/PHY Crossing

- Timing closure must account for multiple factors
  - Clock path OCV
  - Subsys clock jitter
  - PLL clock jitter/delay
  - Process uncertainty
  - Flop margin
  - Datapath length
- Higher data rates can affect the choice of controller/PHY frequency ratio
  - 1:1
  - 1:2
  - 1:4

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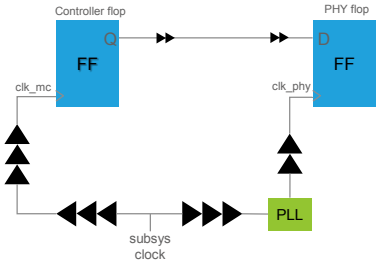
Design Challenges—Controller/PHY Crossing

- Timing closure must account for multiple factor
- Experience shows PHY level clock tree for this width is ~1ns
  - Includes clock tree buffers and routing delay



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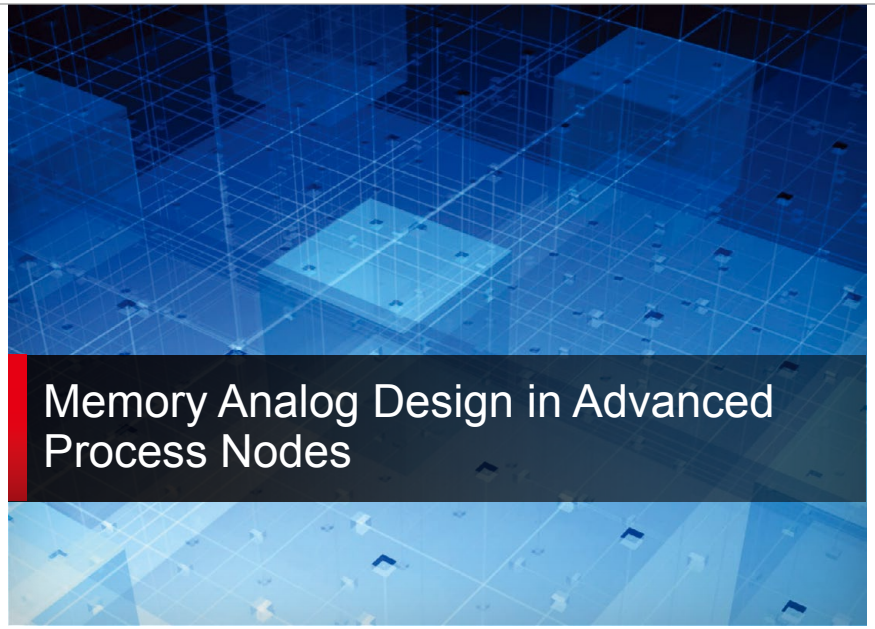
Design Challenges—Voltage/Temperature Variations

- Voltage and temperature can impact calibration results
  - As frequencies increase, VT changes can have a larger impact
  - Affect timing placement/budget
  - Affect impedance
- Monitoring of voltage/temperature changes is necessary
  - Internal adjustments made based on these changes
  - Minimize the disruption while adjustments are made



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Multi-Protocol DDR I/Os

- DDRIO IP *market* would like to have a one-size-fits-all product
  - Supercombo
  - DDR3, DDR3L, DDR4, LPDDR3, LPDDR4, LPDDR4X
- DDRIO IP *users* would like to have an application-optimized solution
  - Mobile, server, consumer, IoT applications
  - POP, memory down, and DIMM configurations
- Some analog design challenges stand in the way of a single DDRIO solution optimized for all applications

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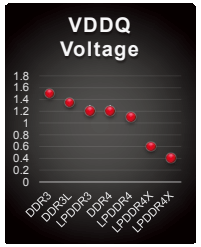
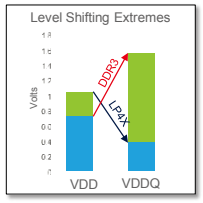
Analog Design Challenges
Supply voltage range

- DDR and LPDDR standards require a wide range of I/O supply voltages (VDDQ)
- Wide supply range drives device selection and circuit topology
  - I/O devices have low gain and high thresholds at 1.06V -40C
  - Speeds of 4266M can't be achieved by I/O devices alone with such a low overdrive voltage
  - Core devices need complex topologies to survive at 1.65V
- Level-shifting topology stressed
  - DDR3: Greater than 1:2 up
  - LPDDR4X: Greater than 2:1 down





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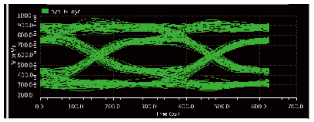
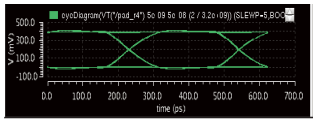
Analog Design Challenges
Impedance and channel equalization

- Different memory configurations: POP, memory down, and DIMMs have different needs
  - Drive and ODT impedance
  - Equalization, crosstalk, and reflections
- Equalization, high driver strength, and high driver linearity cost, power, and area
- DDR3/4 DIMM applications need high driver linearity and strength for multi-rank, sockets, and board loss
- POP and memory down LPDDR applications have short channels and don't need equalization technique

Multi-DIMM DDR4



POP LPDDR4



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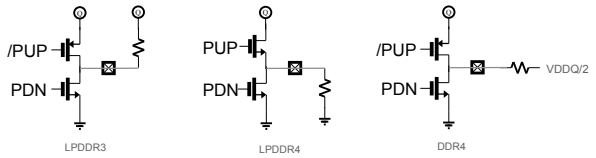
Analog Design Challenges
Common mode

- Different DDR standards are terminated differently
  - DDR4 is terminated to VDDQ (high termination)
  - LPDDR4 is terminated to VSS (low termination)
  - DDR3 is terminated to VDDQ/2 (center termination)
- Output drive topologies must be limited to structures that can support all these different configurations
- Receiver topologies must support rail-to-rail inputs and a wide variety of input signal common mode voltages



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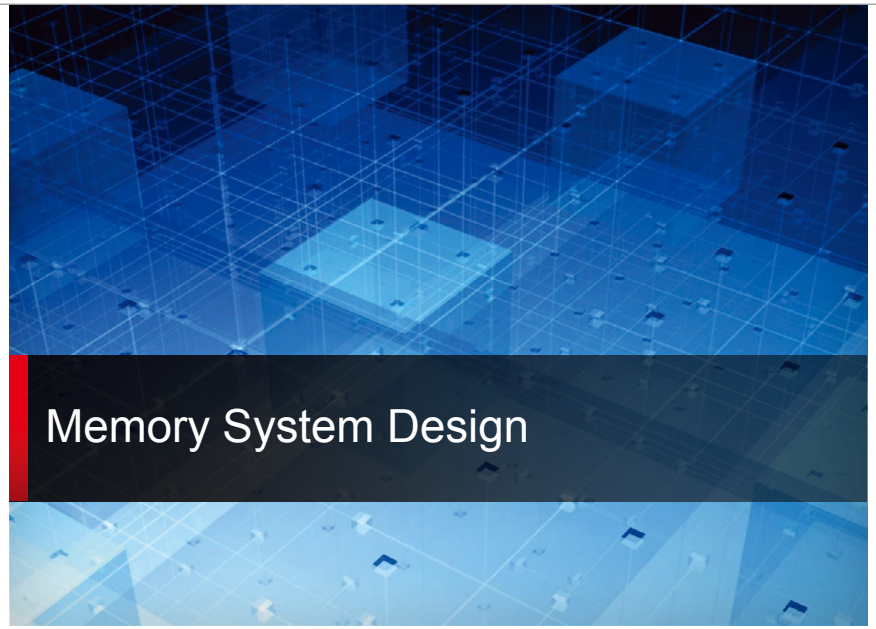

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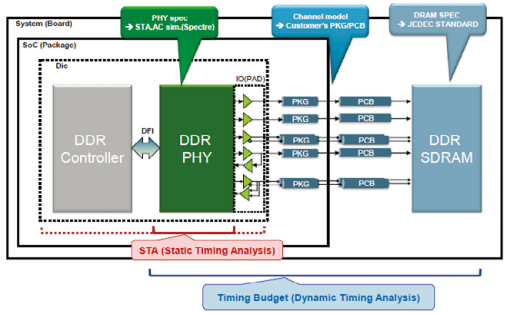
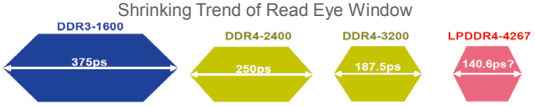
Challenge of High-Speed DDR Timing Budget

Timing Budget Breakdown



Shrinking Trend of Read Eye Window



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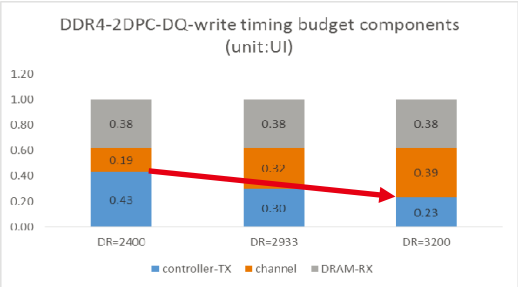
Shrinking Timing Budget for DDR PHY



Controller only gets shrinking piece of the timing budget pie as date rate scales

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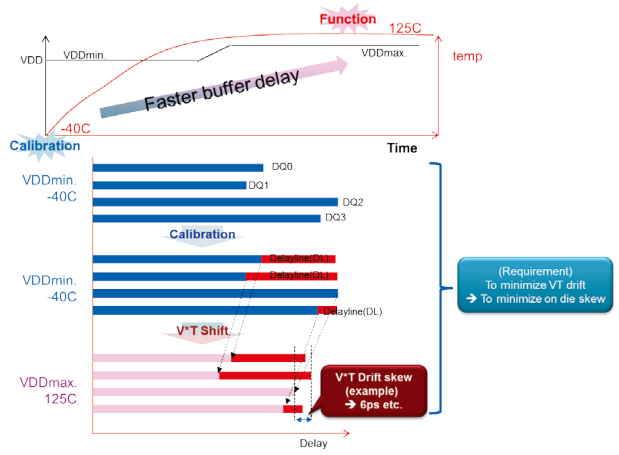
VT Drift Implications on Training and Leveling



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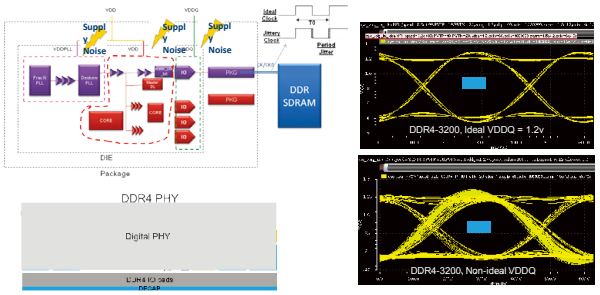
Minimizing Supply Noise to Improve Jitter

- Supply noise induces jitter along the clock or datapath across multiple voltage domains
- Clock or data jitter consumes timing budget, which means running the bus at lower speed



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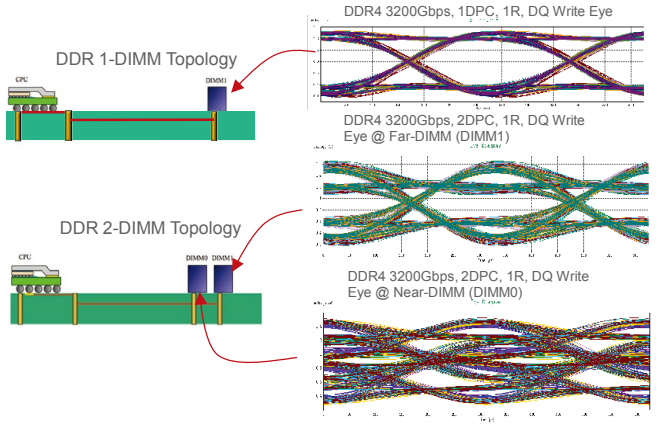
SI Challenges—1DIMM vs. 2DIMM



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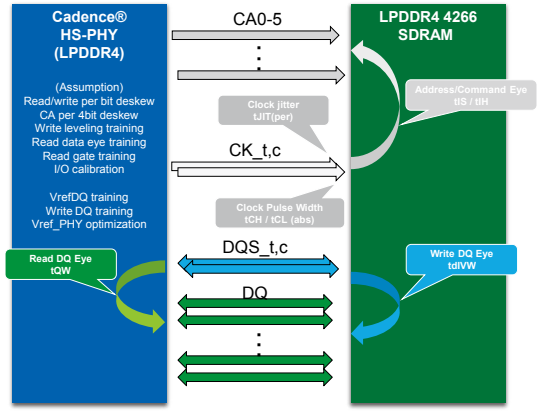
Critical Timing on LPDDR4 @ 4266Mbps



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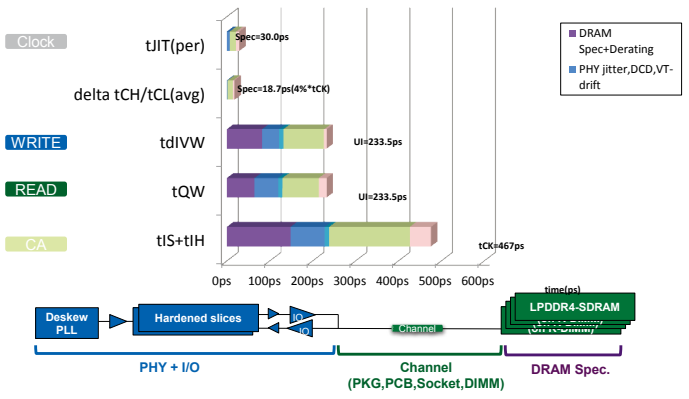
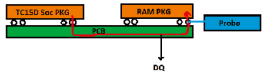
Timing Budget on LPDDR4 @ 4266Mbps

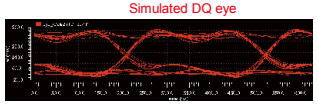
@WC analysis



T16FF+ LP4-Discrete 3.2Gbps Silicon Correlation

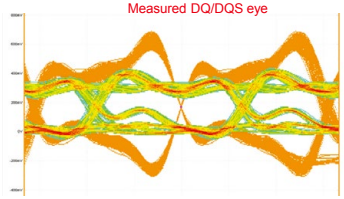


Simulated DQ eye



Cadence T16FF+ LP4-DSC Test Board

Measured DQ/DQS eye



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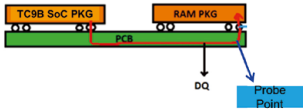
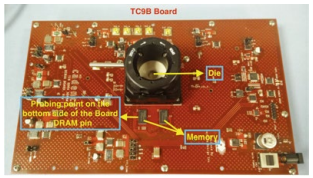
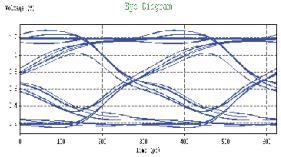
T16FF+ DDR4 Discrete 3.2Gbps Silicon Correlation

Test setup and the probing point

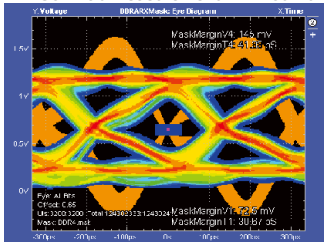




Simulated Eye



TC9B Lab Measurement - 72-hour run



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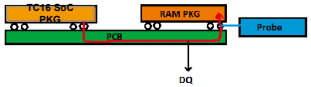
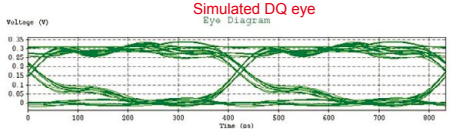
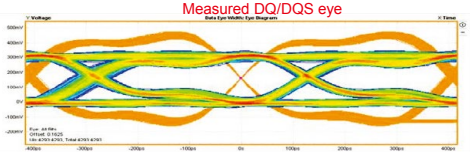
T28HPC LPDDR4 Discrete 2.4Gbps Silicon Correlation



Simulated DQ eye



Measured DQ/DQS eye



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Summary

- DDR design challenges
  - Low power, especially leakage
  - Levelling
  - Controller/PHY crossing
- Flexible analog components supporting multiple protocols
  - Multi-protocol I/Os
  - Supply voltage range
  - Impedance and channel equalization
- With higher data rates, it is necessary to have a system-level view
  - Scalable architecture and training algorithms
  - System timing budget
  - Correlation between simulation and silicon results

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